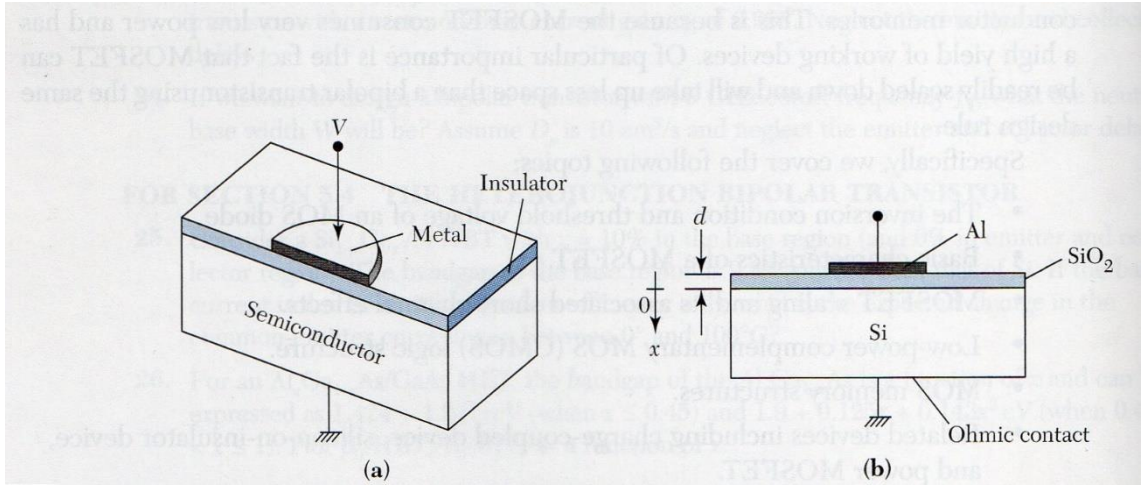
Solid state physics for Nano

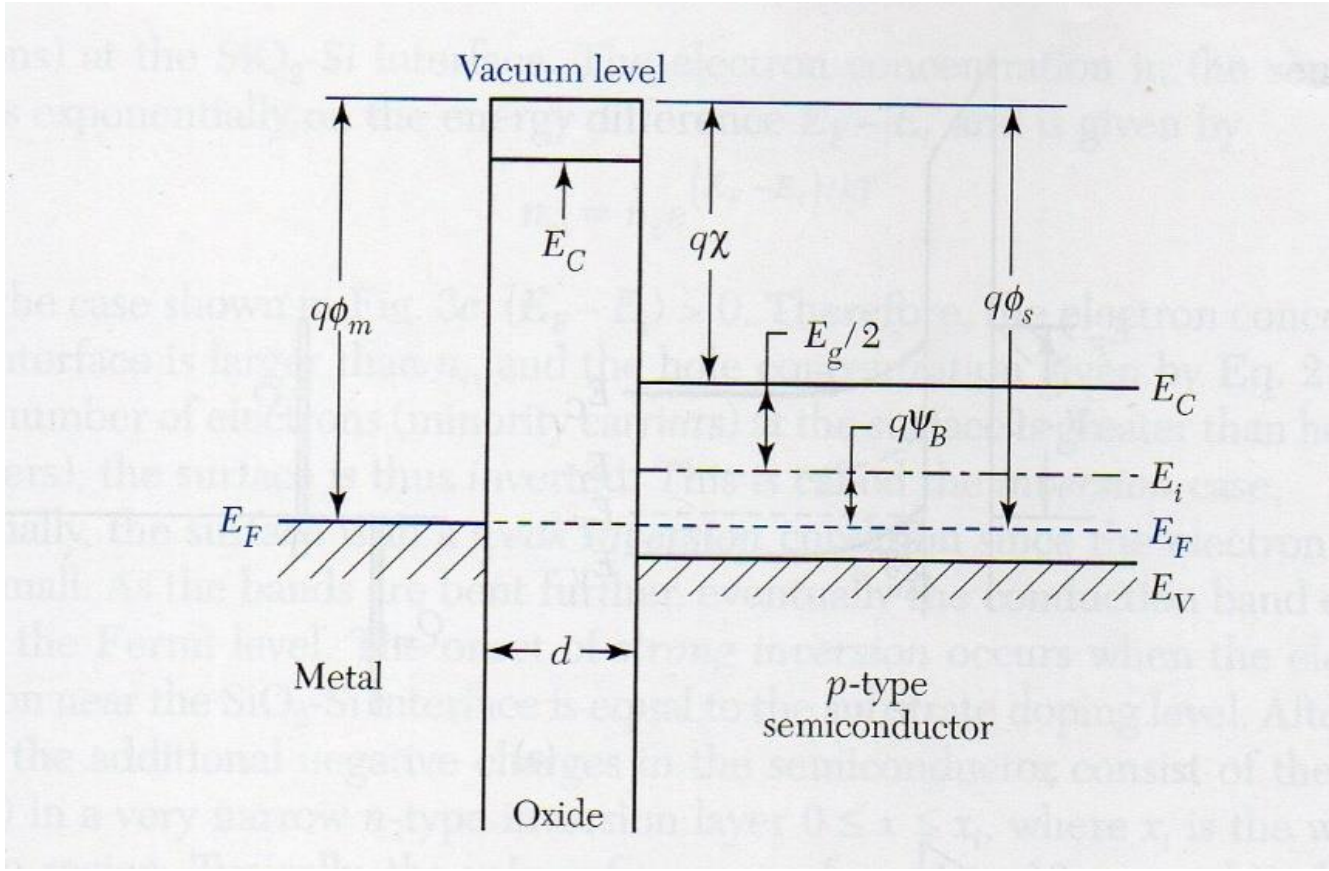
Lecture 8: semiconductor devices

Prof. Dr. U. Pietsch

Metal to semiconductor interface

Basis of MOS diode





Ideal MOS a zero bias

$$q\Phi_{ms} = (q\Phi_m - q\Phi_s) = q\Phi_m - (q\chi + \frac{E_g}{2} + q\psi_B) = 0$$

Accumulation

deplation

Inversion

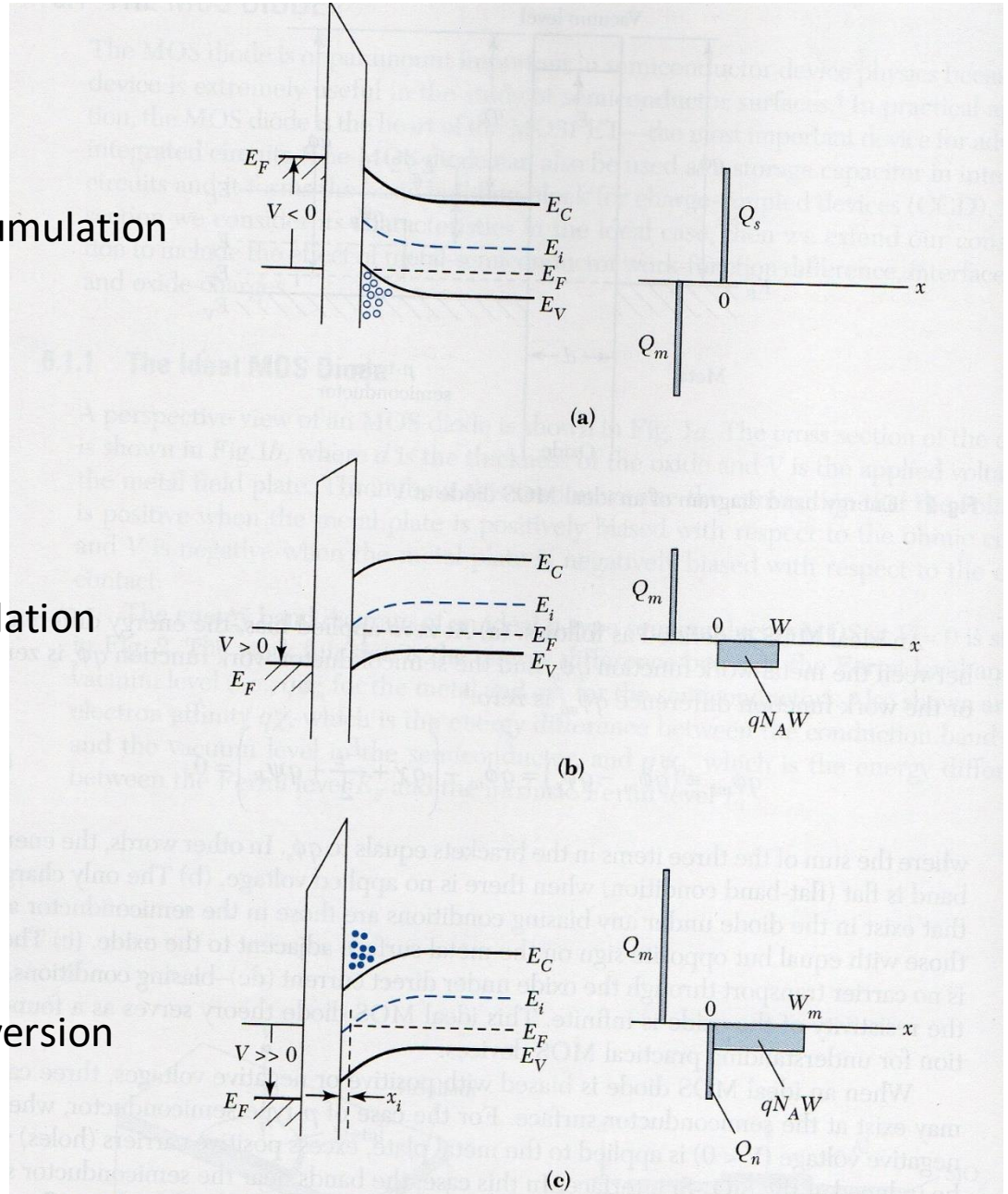


Fig. 3 Energy band diagrams and charge distributions of an ideal MOS diode in (*a*) accumu tion, (*b*) depletion, and (*c*) inversion cases.

Ideal MOS biased, p-type SC

Negative bias (V<0): positive excess carriers (holes) will be induced at SiO_2- Si IF, bands near SC surface bent upwards, no current flow – therefore E_F in SC keeps constant, because

$$p_p = n_i e^{(E_i - E_F)/kT}$$

Pp increases at interface due to bending
Q_s positive charge in SC – Q_m negative charge in metal

If V>0, energy bands in SC bent downwards, majority charriers (holes) are depleted, results in space charge (per unit area) $Q_{sc} = -q\ N_A\ W$

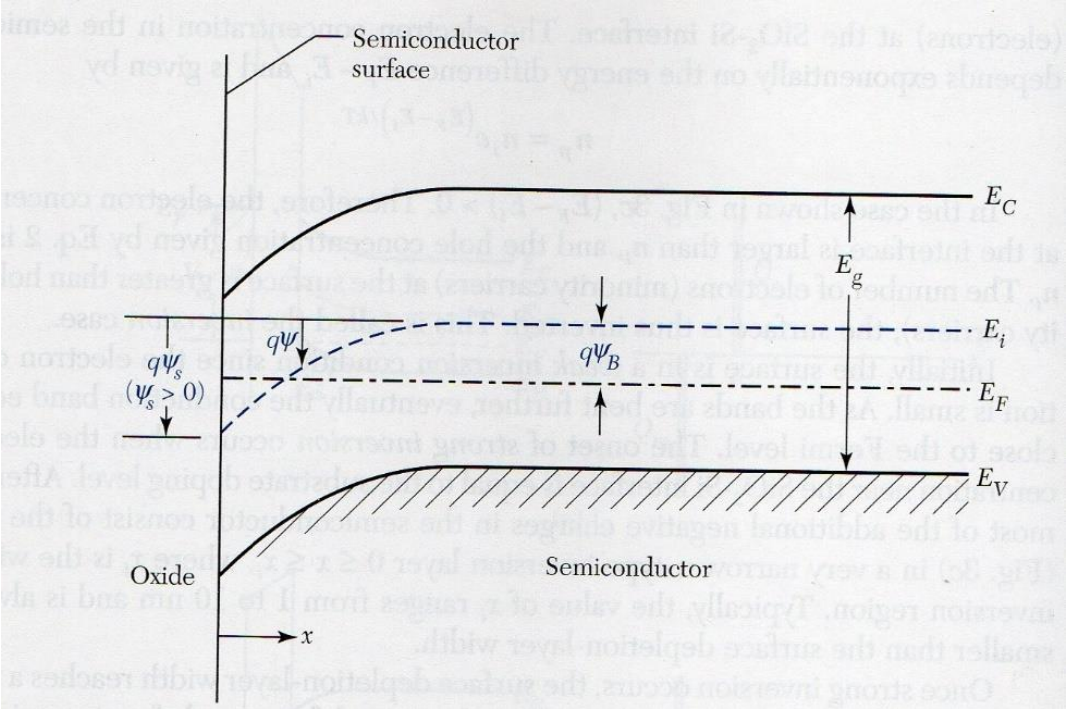
If V>>0, energy bands in SC bent downwards more, so that intrinsic level E_i crosses E_F, → positive gate voltage induces excess negative carrieres (electrons)

$$n_p = n_i e^{(E_F - E_i)/kT}$$

Since E_F-E_i >0 n_p at IF is larger than n_i, d.h. minority carrier at surface are larger than holes (majority)

$$Q_s = Q_n + Q_{sc} = Q_n - qN_AW_m$$

Depletion region



Electrostatic potential $\psi = 0$ in bulk, at surface $\psi = \psi_s$ = surface potential, in terms of ψ, n and p are:

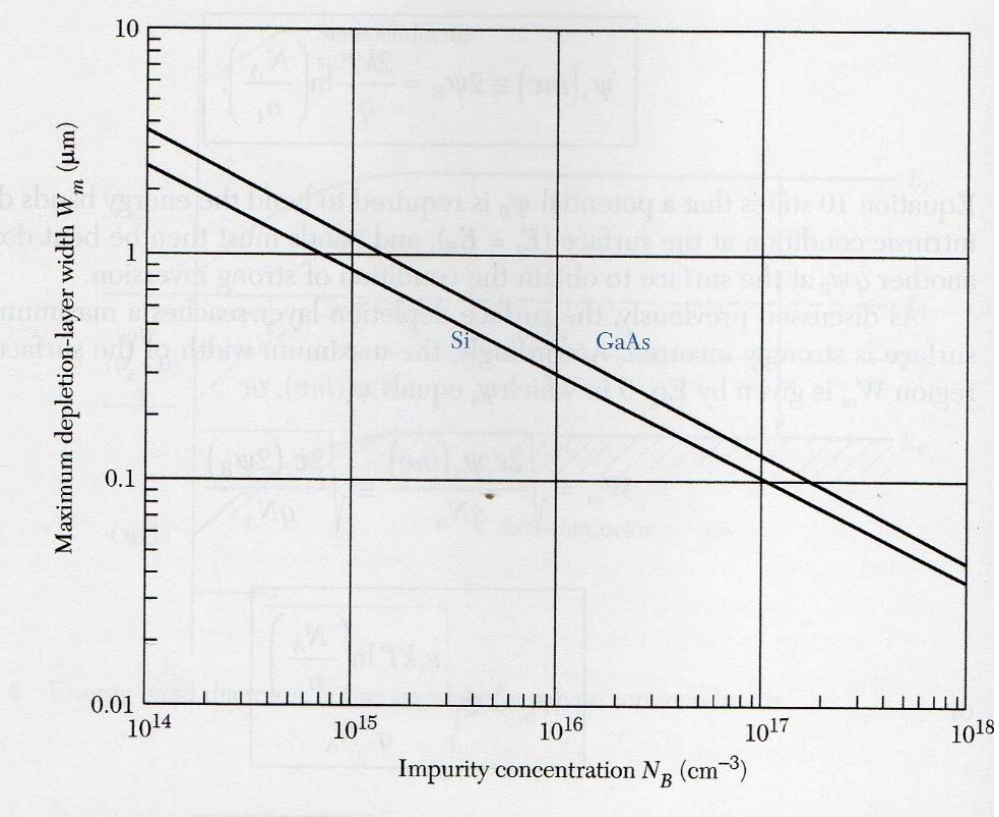
$$n_p = n_i e^{q(\psi - \psi_B)/kT}; \; p_p = n_i e^{q(\psi_B - \psi)/kT}$$

ψ is positive if band bent downwards, at surface carrier density is:

$$n_s = n_i e^{q(\psi_s - \psi_B/kT} \; ; p_s = n_i e^{q(\psi_B - \psi_s)/kT}$$

$\psi_s < 0$ – accumulation of holes
$\psi_s = 0$ – flat band condition
$\psi_B > \psi_s > 0$ – depletion of holes
$\psi_B = \psi_s$ – midgap with $n_s = n_p = n_i$
$\psi_s > \psi_B$ - inversion (bands bent downwards)

Width of depletion region



Depletion width vs doping concentration

$$\frac{d^2\psi}{dx^2} = \frac{-\rho_s(x)}{\varepsilon_s}$$

With $\rho_s = -qN_A$

$$\psi = \psi_s(1 - \frac{x}{W})^2 \qquad \psi_s = \frac{qN_AW^2}{2\varepsilon_s} \quad *$$

$$\psi_s(inv) \cong 2\psi_B = \frac{2kT}{q} ln \frac{N_A}{n_i} \quad **$$

Ψs is required to bend the energy bands down to the intrincic condiion at the surface E_i=E_F. Then bands must be bent downwards by another $q\Psi_B$ at the surface to achieve inversion. Using (*) W (max) is given by

$$W_m = \sqrt{\frac{2\varepsilon_s\psi_s(inv)}{qN_A}} = \sqrt{\frac{2\varepsilon_s(2\psi_B)}{qN_A}}$$

Or using (**)

$$W_m = 2\sqrt{\frac{\varepsilon_s kT ln \frac{N_A}{n_i}}{q^2N_A}}$$

$$Q_s = -qN_AW_m \cong -\sqrt{2q\varepsilon_sN_A(2\psi_s)}$$

Alternative approach to derive Debye length

External charges influence a temporal constant space charge close below the surface of a semiconductor. This space charge is maximum at the surface and decays exponentially towards the bulk - Debye length

Supposing G=U=0 and d/dt=0 $$divj_n = 0$$

Space charge related electric field creates a drift current, which has to be compensated by diffusion current of opposite sign

$$div(eD_n grad\Delta n) + div(\sigma_n E) = 0$$

$$eD_n divgrad\Delta n + \sigma_n divE = 0$$

using $$divD = \varepsilon divE = \rho$$

$$-D_n \frac{d^2\Delta n}{dz^2} + \frac{\sigma_n \rho}{\varepsilon} = 0$$

$$\rho = \rho_0 e^{-z/W}$$

Debye length $$W = \sqrt{\frac{\varepsilon D_n}{\sigma_n}} = \sqrt{\frac{\varepsilon kT}{e^2 n}} \propto \sqrt{\frac{1}{n}}$$

nSC, n= doping conc.

Ideal Metal – Oxide- Semiconductor (MOS) curve

Metal and semiconductor separated by insulator layer

In absense of work function difference the applied voltage will appear partly across the oxide and partly across the SC.

$$V = V_0 + \psi_s \qquad V_0 = E_0 d = \frac{|Q_s|d}{\varepsilon_{ox}} = \frac{|Q_s|}{C_0}$$

V_0 is the potential across the oxide

$$C = \frac{C_0 C_j}{C_0 + C_j} \qquad C_j = \varepsilon_s / W_m \qquad \frac{C}{C_0} = \frac{1}{\sqrt{1 + \sqrt{\frac{2\varepsilon_{ox}^2 V}{qN_A \varepsilon_s d^2}}}}$$

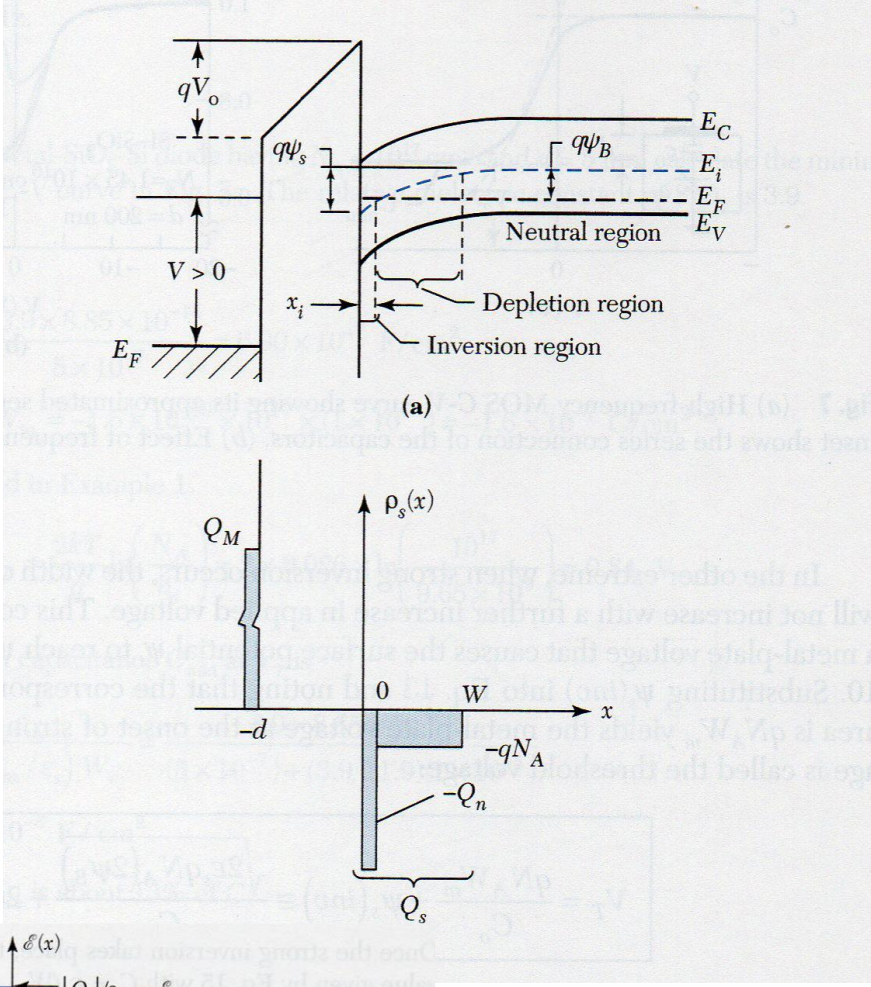
C decreases with increasing V, at inversion C is minimum

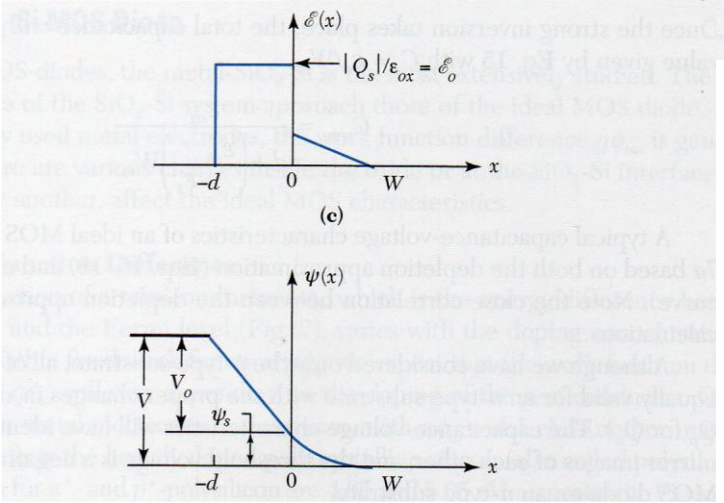
Metal-plate voltage measuring onset of strong inversion

$$V_T = \frac{qN_A W_m}{C_0} + \psi_s(inv)$$

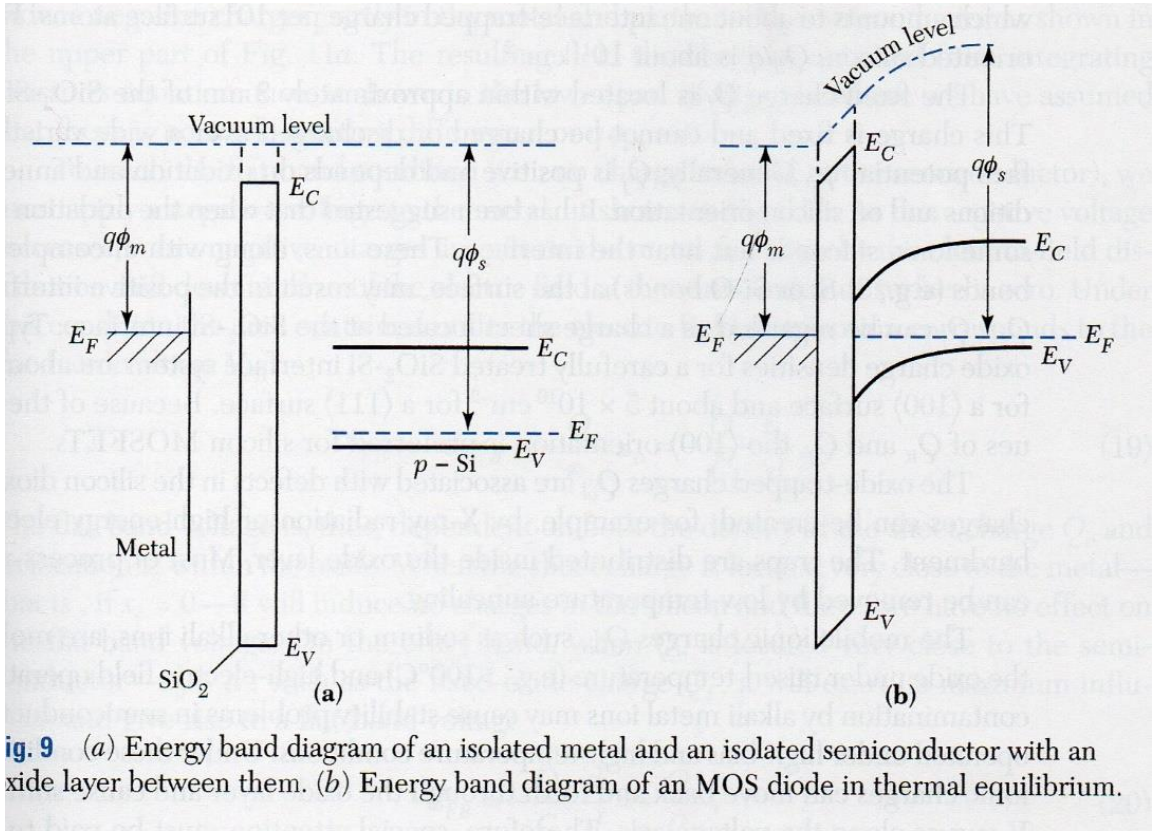
C = C_{min} at inversion

$$C_{min} = \frac{\varepsilon_{ox}}{d + (\varepsilon_{ox}/\varepsilon_s)W_m}$$





SiO_2 – Si MOS diode



ig. 9 (*a*) Energy band diagram of an isolated metal and an isolated semiconductor with an xide layer between them. (*b*) Energy band diagram of an MOS diode in thermal equilibrium.

Work function difference:

$$q\varphi_{ms} = (q\varphi_m - q\varphi_s)$$

q ϕ_m (Al) = 4.1eV, q ϕ_s (Si) = 4.05..5.05eV,
q ϕ_{ms} can vary from 0.1…2 eV depending on doping

Work function difference has be compensated by negative Volage
$V_{FB} = \phi_{ms}$ →flat band voltage

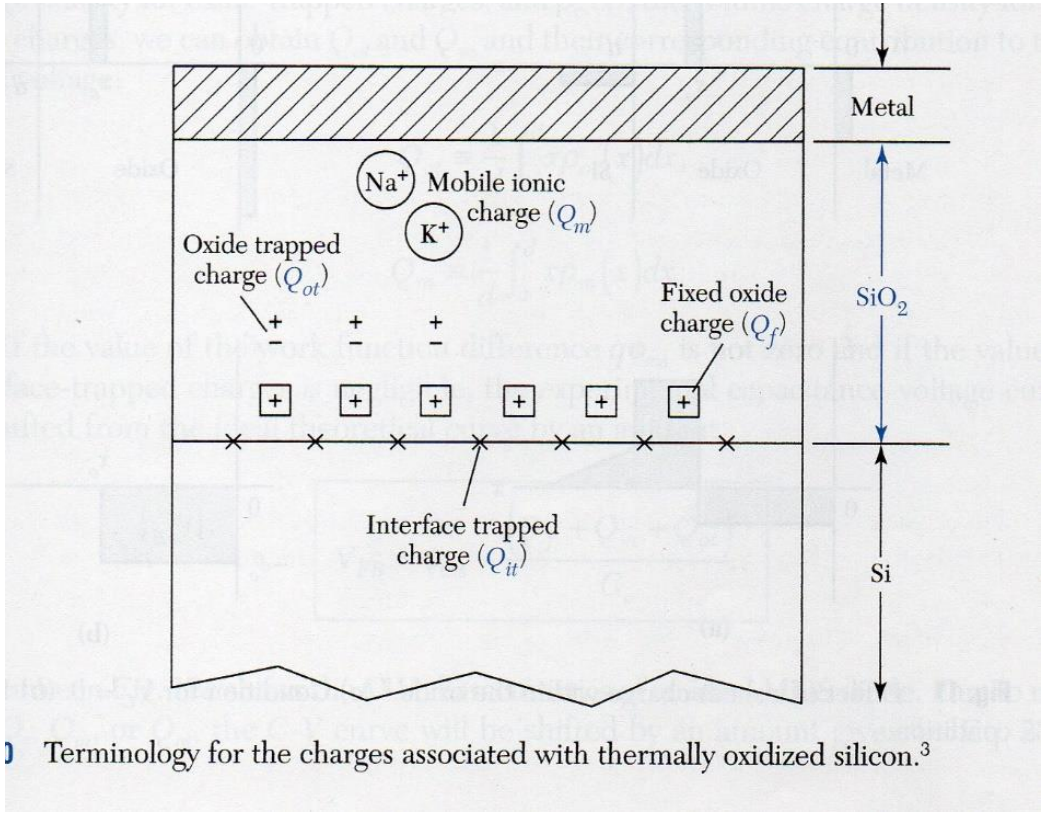
Components of isolated Materials relativ to vacuum level

Components of isolated Materials with continuous Fermienergy

Impact of interface traps and oxid charges on flat band voltage

Positive sheet charge in oxide induce negative charges in metal and SC

Flat band condition , there is no charge in SC



Terminology for the charges associated with thermally oxidized silicon.[3]

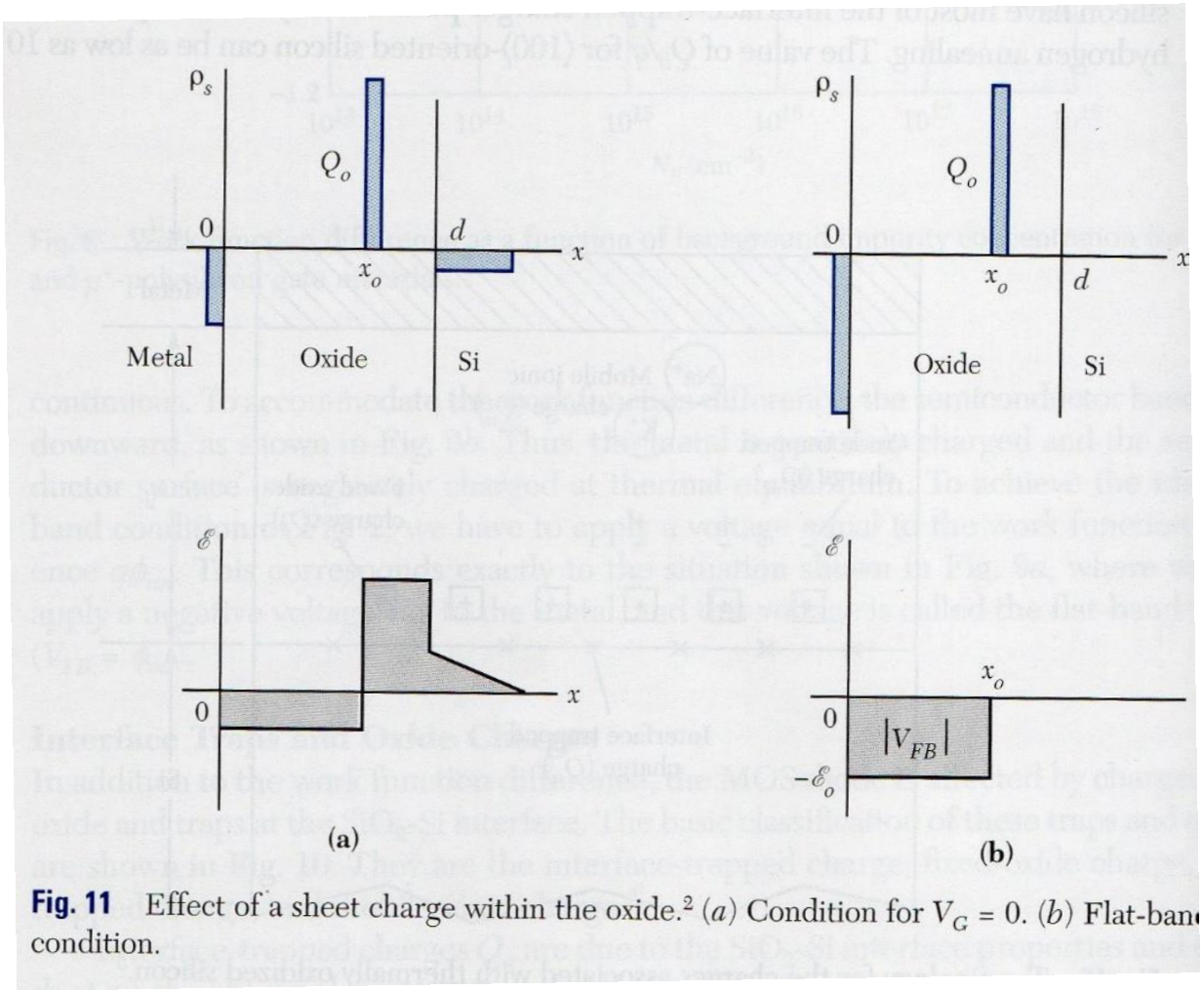
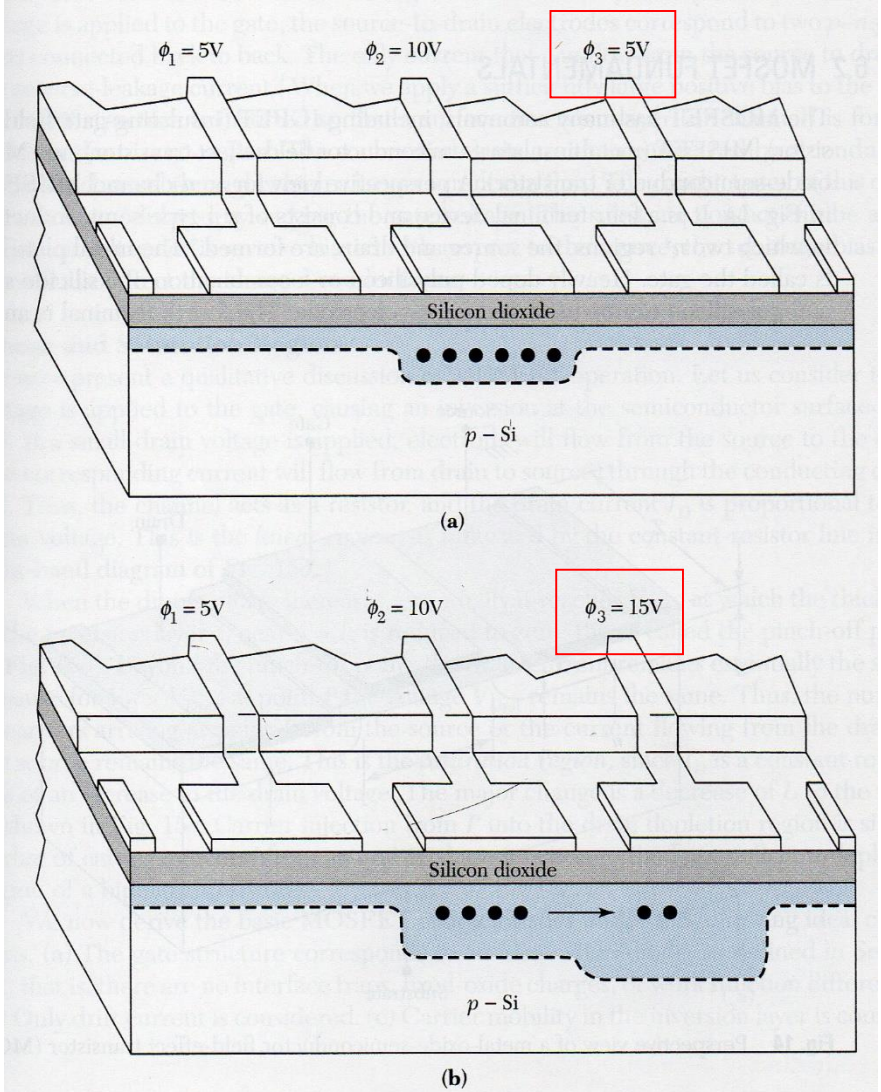


Fig. 11 Effect of a sheet charge within the oxide.[2] (*a*) Condition for $V_G = 0$. (*b*) Flat-band condition.

$$V_{FB} = \varphi_{ms} - \frac{(Q_f + Q_m + Q_{ot})}{C_0}$$

Charge coupled devices CCD



13 Cross section of a three-phase charge-coupled device.[4] (*a*) High voltage on ϕ_2. ϕ_3 pulsed to a higher voltage for charge transfer.

Transfer of charge charriers below the gate of one pixel to the neighboured pixel

MOSFET fundamentals

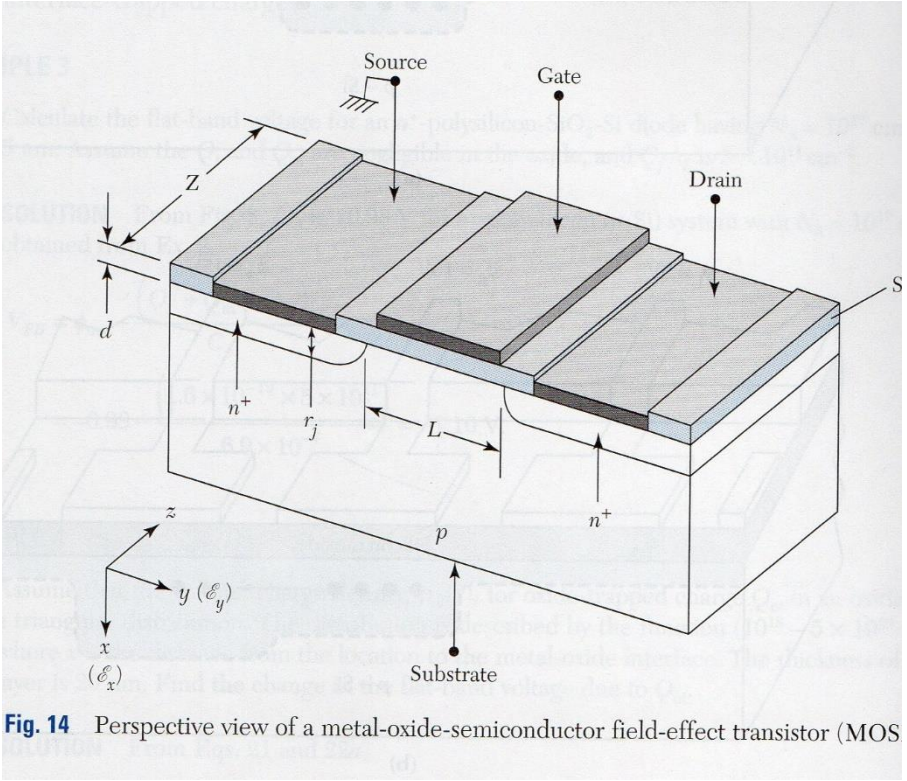
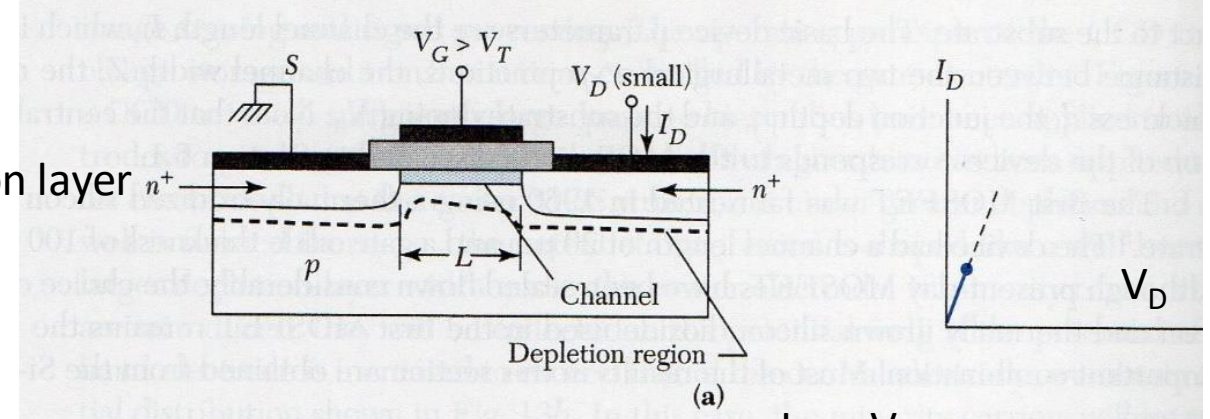
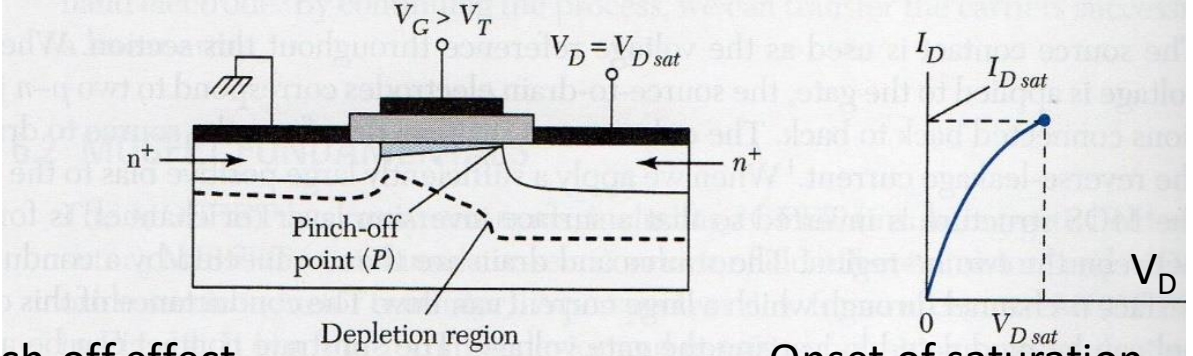


Fig. 14 Perspective view of a metal-oxide-semiconductor field-effect transistor (MOS

n+ inversion layer



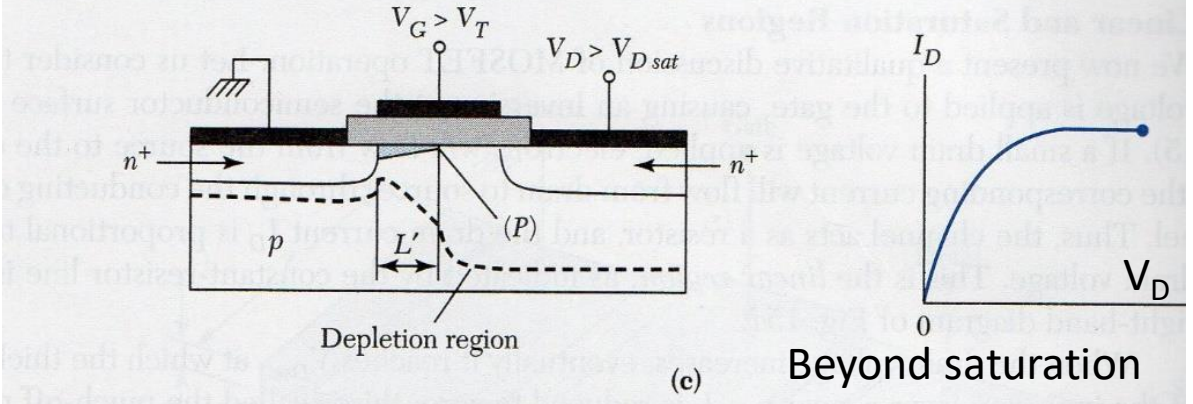
Low V_D



Pinch-off effect

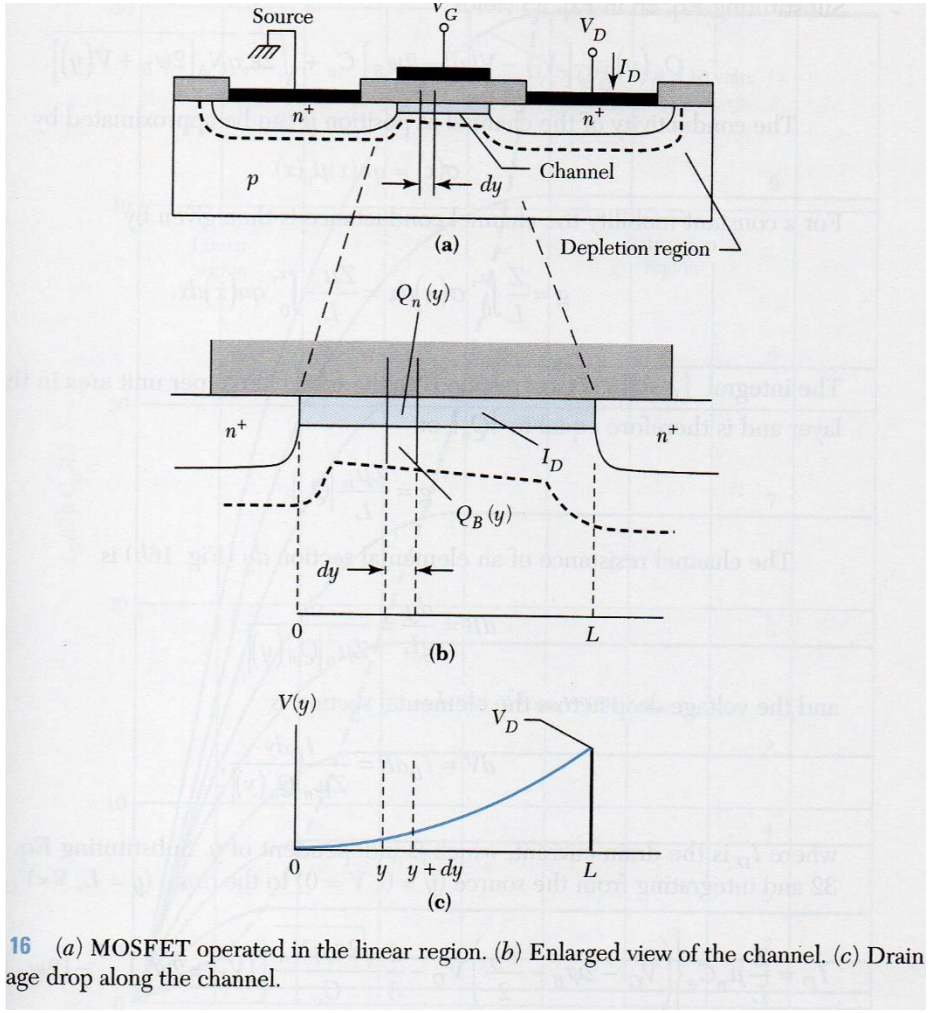
Onset of saturation

$V_{D=}V_{Dsat}$



Beyond saturation

MOSFET operating in the linear region



16 (*a*) MOSFET operated in the linear region. (*b*) Enlarged view of the channel. (*c*) Drain age drop along the channel.

Surface charge Qs as function of distance from source contact

$$Q_s(y) = -[V_G - \psi_s(y)]C_0$$

ψ_s(y) is surface potential at y; $C_0 = \varepsilon_{ox}/d$ gate capacitance

$$Q_n(y) = Q_s - Q_{sc} = -[V_G - \psi_s(y)]C_0 - Q_{sc}(y)$$

ψ_s(y) at inversion is $2\psi_B + V(y)$, V(y) is reverse bias between y nd source electrode, charge within surface depletion region:

$$Q_{sc}(y) = -qN_A W_m \cong -\sqrt{2\varepsilon_s qN_A[2\psi_B + V(y)]}$$

Which gives:

$$Q_n(y) \cong -[V_G - V(y) - 2\psi_B]C_0 + \sqrt{2\varepsilon_s qN_A[2\psi_B + V(y)]}$$

Drain current I_D

$$I_D \cong \frac{Z}{L}\mu_n C_0 (V_G - V_T) V_D \ldots . for \ldots V_D << (V_G - V_T)$$

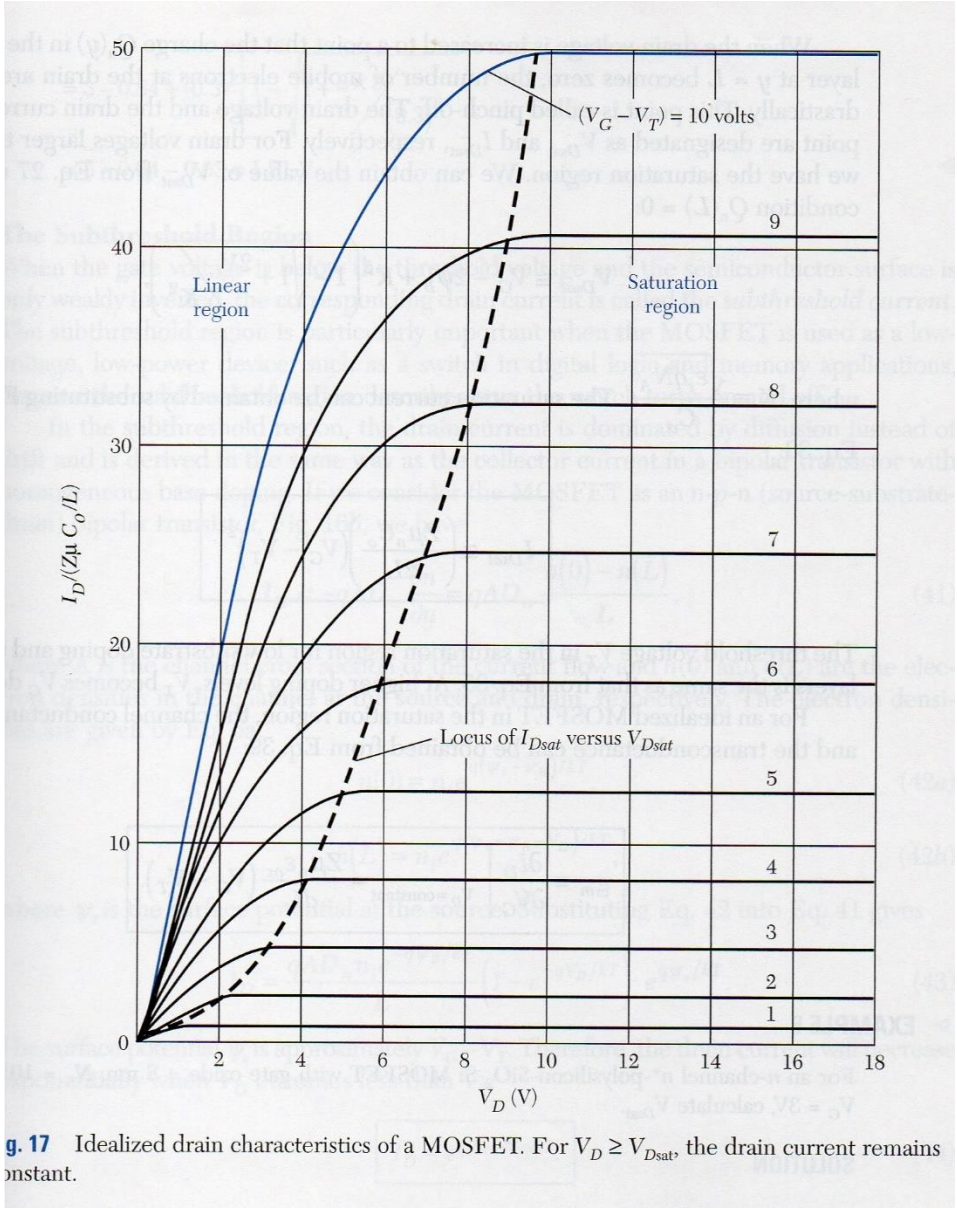
With threshold voltage V_T

$$V_T = \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{C_0} + 2\psi_B$$

$$V_{Dsat} \cong (V_G - 2\psi_B) + K^2\left(1 - \sqrt{1 + 2V_G/K^2}\right)$$

$$K = \frac{\sqrt{\varepsilon_s q N_A}}{C_0}$$

$$I_{Dsat} \cong \frac{Z\mu_n C_0}{2L}(V_G - V_T)^2$$



g. 17 Idealized drain characteristics of a MOSFET. For $V_D \geq V_{Dsat}$, the drain current remains onstant.

Types of MOSFETs

n-channel enhancement
(normally off)

n-channel depletion
(normally on)

p-channel enhancement
(normally off)

p-channel depletion
(normally on)

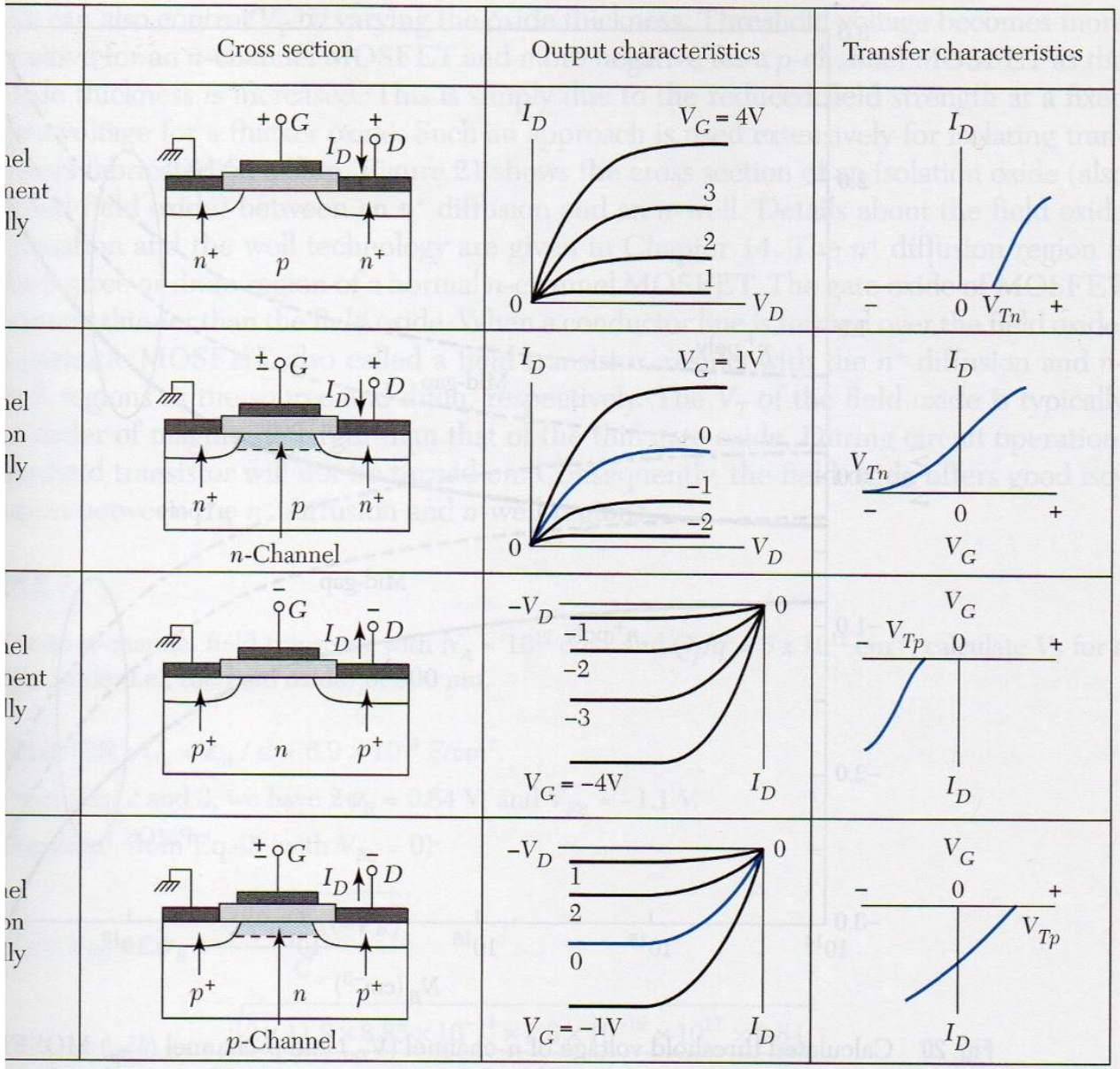
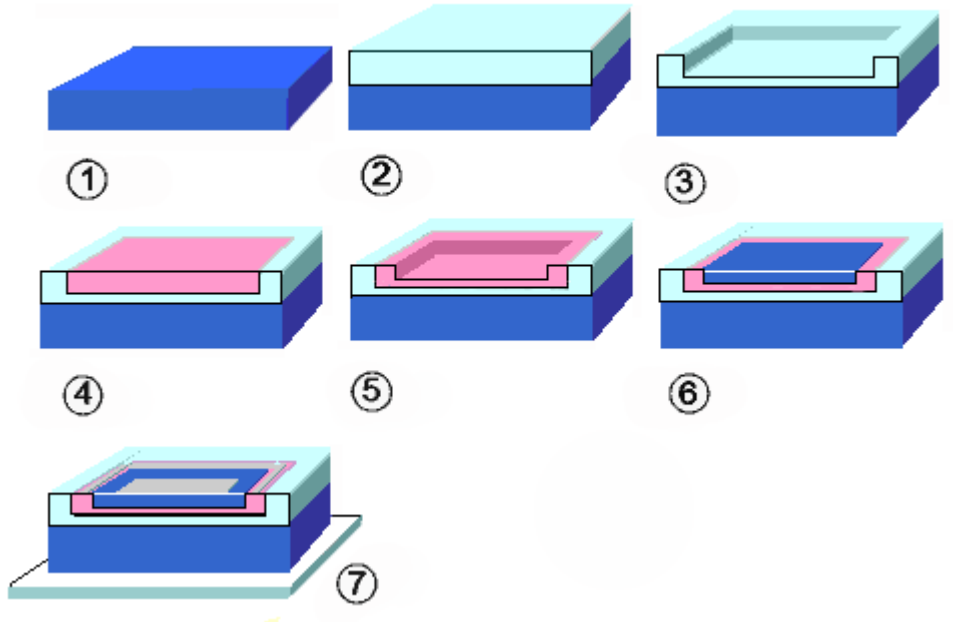
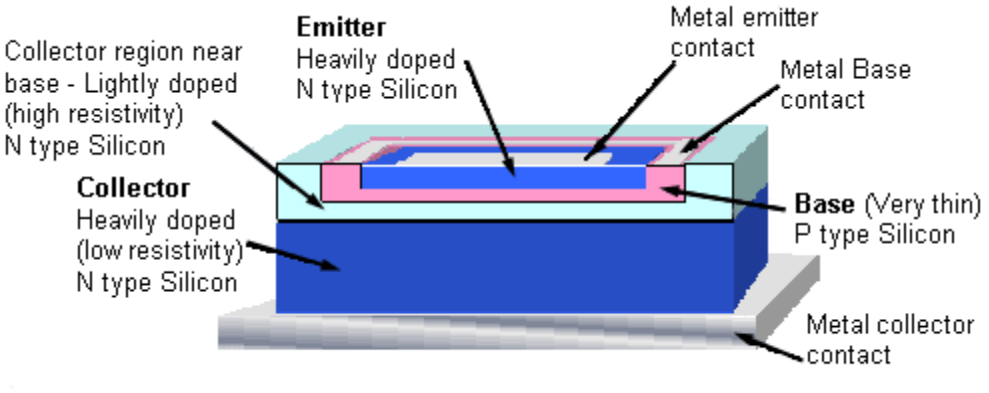


Fig. 19 Cross section, output, and transfer characteristics of four types of MOSFETs.

Silicon device technology

1. Layer 1 - Heavily doped N type Silicon.
2. Lightly doped N type silicon is deposited on top of layer 1 making a two layer collector. (see "How BJTs Work").
3. Part of the collector layer is etched away to form a depression for the P type base layer.
4. P type base layer is added.
5. Part of the base layer is etched away leaving a very thin base layer.
6. A heavily doped N type emitter layer is added.
7. Finally metal connectors are added allowing leads to be fixed after testing, and separating from the wafer.





http://www.learnabout-electronics.org/Semiconductors/